

NanoArc ACE Mira RevA

Annotated Pinmap and Datasheet Reference

Low-voltage ACE controller, panel, analog simulator, and logic-support wiring guide

Scope: This document is a breadboard-friendly and KiCad-friendly reference for the ACE RevA/Mira low-voltage control board. It reconciles the existing pinmap with datasheet-specific wiring notes and the parts that appear in the BOM/invoice set. It is not an output-stage or high-current Weld Energy Stage construction plan. [S13]

Important naming note: Older tables used GND. Current schematic work may use CMN_GND. Pick one ground net name in KiCad and use it everywhere. In this document, CMN_GND means ACE logic ground only.

Document	Purpose
Part 1	How to use this reference, global rules, net names, and bring-up order.
Part 2	Pin-by-pin tables for Nano, I2C/FRAM, MCP23017s, ADC/reference/op-amp, LED drivers, fault logic, keypad, encoder, and protection.
Part 3	Plain-English explanations: pull-ups, pull-downs, open-drain/open-collector, push-pull, decoupling, VREF, NC/DNC, and common ERC errors.
Part 4	Must-connect / optional / leave-open checklists and source references.

Quick Table of Contents

Section	What you use it for
1. Quick rules	Fast default rules before drawing or breadboarding.
2. System map	How the Nano, I2C, SPI, analog reference, fault logic, and panel fit together.
3. Reference designator map	What each U/J/SW/D/BZ ref is for.
4. Pin maps	Detailed per-device wiring tables.
5. Concepts	Pull-up/down, open-drain, push-pull, decoupling, VREF, NC/DNC.
6. KiCad/ERC	How to silence the right warnings and fix real ones.
7. Bring-up order	Breadboard test sequence that avoids debugging everything at once.
8. Source references	Datasheets and uploaded project files used.

1. Quick Rules

These are the rules to keep beside KiCad. If a detailed table later appears to conflict with these, follow the detailed table and then ask *why*.

Topic	Net / part	Rule
Logic rail	+5V_LOGIC	5 V controller rail only. Add 100 uF near the carrier input, plus 10 uF per board/branch and 100 nF at each IC.
Ground	CMN_GND	ACE logic ground. Do not use this as a high-current return for any later output-stage hardware.
I2C	I2C_SDA / I2C_SCL	One pair of pull-ups, normally 4.7 kOhm to +5V_LOGIC. Do not scatter duplicate pull-ups on every board.
Switch inputs	ARM_SW, TRIGGER_SW, etc.	Default HIGH with 10 kOhm pull-up; switch closes to CMN_GND; firmware treats LOW as active.
Open-drain / open-collector	FAULT_SUM, EXPANDER_INT, LMV393 outputs	Needs a pull-up. Devices only pull LOW or let go. Safe for shared interrupt/fault lines.
Push-pull outputs	Ordinary GPIO, 74HC outputs	One driver per net. Do not tie push-pull outputs together.
ADC range	MCP3208 input	Input must stay between CMN_GND and VREF_2V5 when VREF is REF5025.
NC / DNC	REF5025 DNC, MCP23017 NCs	Mark as No Connect in KiCad unless the datasheet explicitly permits another treatment.
Unused CMOS inputs	74HC inputs, op-amp/comparator inputs	Never float. Tie to a defined rail or bias into a safe state.
Long schematic wires	Across-page nets	Use labels for long-distance buses, visible local wires inside each functional block

Safety scope: Nets named PULSE_CMD, CHARGE_ENABLE, BLEED_ENABLE, and machine I/O are low-voltage simulator/control nets only in this document. No high-current wiring is specified here.

2. System Map

```
Nano Every
|  -- I2C: A4=SDA, A5=SCL
|      |  -- U2 FRAM breakout, default 0x50
|      |  -- U3 MCP23017 panel input, 0x20
|      |  -- U4 MCP23017 panel output, 0x21
|      |  -- U5 MCP23017 machine I/O simulator, 0x22
|
|  -- SPI: D11=MOSI, D12=MISO, D13=SCK, D10=ADC_CS
|      |  -- U6 MCP3208 ADC
|
|  -- Direct safety/control pins
|      |  -- FAULT_SUM, TRIP_OV, ARM_SW, HARD_SAFE_SW, GRIP_SW,
|          TRIGGER_SW, OUTPUT_FB, PULSE_CMD, HW_INHIBIT,
|          CHARGE_ENABLE, ENCLOSURE_INTLK, EXPANDER_INT,
|          HANDPIECE_PRESENT, TRIP_OC

Analog island
REF5025 -> VREF_2V5 -> MCP3208 VREF and simulator pot top rail
MCP6004 -> optional buffers for temp/sensor simulator inputs

Panel output
MCP23017 outputs -> ULN2803A inputs -> LED chains / optional buzzer driver
```

3. Reference Designator Map

Ref	Part	Circuit role	Datasheet / KiCad note
U1	Arduino Nano Every ABX00028	ACE controller brain: direct pins, I2C, SPI, serial diagnostics.	Use Nano module symbol or two 1x15 sockets. [S1]
J1/J2	Samtec 1x15 sockets	Removable Nano Every sockets.	Physical assembly aid. [S13]
U2	Adafruit 1895 I2C FRAM breakout	Persistent storage module.	Use breakout symbol, not bare FRAM chip. [S10]
U3	MCP23017-E/SP	Panel input expander at 0x20.	Keypad, encoder, panel-present. [S2]
U4	MCP23017-E/SP	Panel output expander at 0x21.	Talkback command nets and panel outputs. [S2]
U5	MCP23017-E/SP	Machine I/O / loopback expander at 0x22.	Low-voltage simulator only. [S2]
U6	MCP3208-CI/P	8-channel SPI ADC.	External ADC for analog simulator channels. [S3]
U7	REF5025AID	2.5 V precision ADC reference.	SOIC-8; needs adapter for breadboard. [S4]
U8	MCP6004-I/P	Quad op-amp buffer/filter.	PDIP-14. Bias unused channels. [S5]
U9	ULN2803A	Low-side sink driver.	LED chains and possibly other low-current loads. [S9]
U10	SN74HC573AN	Fault-source latch / diagnostic capture.	Define OE and LE. [S8]
U11	CD74HC221E	Logic-only timing/window fixture.	Unused inputs must not float. [S7]
U12-U14	LMV393IDR	Comparator channels.	Open-collector outputs need pull-ups. [S6]
D1-D8	3 mm white LEDs	Talkback indicators.	+5V -> resistor -> LED -> ULN output. [S13]
BZ1	PUI 5 V buzzer	Audible feedback.	Use separate driver if all ULN channels are occupied. [S13]
SW1-SW20	TL1105 tactile switches	4x5 keypad matrix.	Four-pin switch: same-side pins tied together.
ENC1	PEC11R encoder	Rotary input and push switch.	Use pull-ups and debounce. [S11]

4. Pin Maps and Wiring Tables

4.1 U1 Arduino Nano Every direct pin map

This follows the existing Mira pinmap intent, with direct pins reserved for signals that should not be hidden behind I2C. The exact firmware assignment can still change, but these are the working schematic names. [S1][S13]

Pin	Net	Dir	Connects to	Default / resistor	Note
D0/RX	UART_RX	In	Service UART/USB serial	Reserved; no external pull	Serial debug while OLED is deferred.
D1/TX	UART_TX	Out	Service UART/USB serial	Reserved; no external pull	Do not spend on panel I/O.
D2	FAULT_SUM	In	Fault aggregation node	10 k pull-up; active LOW	Direct critical summary.
D3	TRIP_OV	In	Comparator/latch output	Pull-up if open-collector; active LOW	Over-limit simulator.
D4	ARM_SW	In	ARM toggle to ground	10 k pull-up; active LOW	Direct panel control.
D5	HARD_SAFE_SW	In	Hard-safe switch to ground	10 k pull-up; active LOW	Do not put behind I2C.
D6	GRIP_SW	In	Grip sim switch/jumper	10 k pull-up; active LOW	Bench simulator.
D7	TRIGGER_SW	In	Trigger sim switch/jumper	10 k pull-up; active LOW	Bench simulator.
D8	OUTPUT_FB	In	Low-voltage feedback sim	10 k pulldown if source can float	No energized output feedback.
D9	PULSE_CMD	Out	Test LED/header or U11 only	100 k pulldown at fixture; optional 1 k series	No energy-stage connection in RevA.
D10	ADC_CS	Out	MCP3208 CS/SHDN	10 k pull-up optional	SPI chip select.
D11	SPI_MOSI	Out	MCP3208 DIN	Optional 100 ohm series	SPI data to ADC.
D12	SPI_MISO	In	MCP3208 DOUT	No pull normally	SPI data from ADC.
D13	SPI_SCK	Out	MCP3208 CLK	Optional 100 ohm series	SPI clock.
A0	HW_INHIBIT	Out	Low-voltage inhibit/test header	100 k pulldown at fixture	Safe-default low.
A1	CHARGE_ENABLE	Out	Test LED/header only	100 k pulldown; 1 k if LED used	Simulator only.
A2	ENCLOSURE_INTLK	In	Interlock jumper to ground	10 k pull-up; active LOW	Direct interlock.
A3	EXPANDER_INT	In	MCP23017 INTA/INTB open-drain shared line	10 k pull-up; active LOW	Do not tie push-pull INTs together.
A4	I2C_SDA	Bi	FRAM and MCP23017 SDA	4.7 k pull-up to +5V	Shared I2C bus.
A5	I2C_SCL	Out	FRAM and MCP23017 SCL	4.7 k pull-up to +5V	Shared I2C bus.
A6	HANDPIECE_PRESENT	In	Presence jumper/header	10 k pull-up; jumper to ground active LOW	Bench presence sim.
A7	TRIP_OC	In	Comparator/latch output	Pull-up if open-collector; active LOW	Over-current simulator.

4.2 I2C backbone and U2 FRAM breakout

Use one I2C trunk and branch to each device. The Adafruit FRAM breakout defaults to address 0x50. Address pins A0/A1/A2 can change the low address bits; power-cycle after strap changes. WP has an internal pulldown and only write-protects when pulled high. [S10]

From	Net	Purpose	Passive/default	Note
U1 A4	I2C_SDA	I2C data trunk	4.7 k to +5V_LOGIC	One pull-up pair on ACE carrier.
U1 A5	I2C_SCL	I2C clock trunk	4.7 k to +5V_LOGIC	One pull-up pair on ACE carrier.
U2 VCC	+5V_LOGIC	FRAM breakout power	100 nF local if on carrier	Breakout accepts 3-5 V.
U2 GND	CMN_GND	FRAM ground	None	Common logic ground.
U2 SCL	I2C_SCL	FRAM clock	Uses bus pull-up	Do not add a second strong pull-up unless needed.
U2 SDA	I2C_SDA	FRAM data	Uses bus pull-up	Shared bus.
U2 WP	FRAM_WP or CMN_GND	Write protect	Tie low for normal writes	May be controlled later if needed.
U2 A0/A1/A2	CMN_GND unless moved	I2C address bits	Tie low for 0x50	Do not leave floating if represented in schematic.

MCP23017 common pin map

DIP pin	Name	Function	Mira rule	
1-8	GPB0-GPB7	GPIO	Assign per U3/U4/U5 role. Inputs may use internal weak pull-ups; external 10 k preferred for off-board wiring.	
9	VDD	Power	+5V_LOGIC with 100 nF to CMN_GND nearby.	
10	VSS	Ground	CMN_GND.	
11	NC	No connect	Leave open; mark No Connect.	
12	SCL	I2C clock	I2C_SCL.	
13	SDA	I2C data	I2C_SDA.	
14	NC	No connect	Leave open; mark No Connect.	
15	A0	Address bit 0	Strap high/low; never float.	
16	A1	Address bit 1	Strap high/low; never float.	
17	A2	Address bit 2	Strap high/low; never float.	
18	RESET	Active reset	Pull up to +5V_LOGIC through 10 k. Optional reset switch to ground.	
19	INTB	Interrupt output	Use open-drain if sharing EXPANDER_INT.	
20	INTA	Interrupt output	Use open-drain if sharing EXPANDER_INT.	
21-28	GPA0-GPA7	GPIO	Assign per U3/U4/U5 role.	
Device		Address	Address strap	Role
U3 panel input		0x20	A2=0, A1=0, A0=0	Key matrix, encoder, panel-present.
U4 panel output		0x21	A2=0, A1=0, A0=1	Talkback/ULN command outputs and panel controls.
U5 machine I/O sim		0x22	A2=0, A1=1, A0=0	Low-voltage loopback and status simulator only.

4.3 MCP23017 role overlays

These are the preferred logical allocations. The exact KiCad placement can remain one sheet, but the net names should stay consistent.

U3 pins/port	Net	Rule
GPA0-GPA4	KPD_COL0-KPD_COL4	Keypad column lines. Prefer visible bus/wires in schematic.
GPA5-GPA7	KPD_ROW0-KPD_ROW2	Keypad row lines.
GPB0	KPD_ROW3	Fourth keypad row.
GPB1	ENC_A	Encoder quadrature A; pull-up; debounce in firmware.
GPB2	ENC_B	Encoder quadrature B; pull-up; debounce in firmware.
GPB3	ENC_SW	Encoder push switch; pull-up, active LOW.
GPB4	PANEL_PRESENT	Jumper or detect line.
GPB5-GPB7	SPARE_IN0-2	Tie or mark intentional spares.
U4 port	Net	Rule
GPA0	TB_SAFE_CMD	To ULN IN1 -> SAFE LED chain.
GPA1	TB_CHARGE_CMD	To ULN IN2 -> CHARGE LED chain.
GPA2	TB_READY_CMD	To ULN IN3 -> READY LED chain.
GPA3	TB_ARMED_CMD	To ULN IN4 -> ARMED LED chain.
GPA4	TB_OUTPUT_CMD	To ULN IN5 -> OUTPUT LED chain.
GPA5	TB_FAULT_CMD	To ULN IN6 -> FAULT LED chain.
GPA6	TB_ENERGY_CMD	To ULN IN7 -> ENERGY LED chain.
GPA7	TB_OPR_ERR_CMD	To ULN IN8 -> OPR ERR LED chain.
GPB0	OLED_RST	Leave unpopulated/deferred if OLED is deferred.
GPB1	BUZZER_CMD	Use separate small driver unless you reserve a ULN channel.
GPB2	LAMP_TEST	Optional logic control.
GPB3	PANEL_DIM_EN	Optional.
GPB4-GPB7	SPARE_OUT	Leave as intentional spares.
U5 port	Net	Rule
GPA0	CHARGER_READY	Low-voltage status simulator input.
GPA1	CHARGER_FAULT	Low-voltage status simulator input.
GPA2	BLEED_CONFIRM	Low-voltage status simulator input.
GPA3	FAN_TACH_OR_GOOD	Status simulator.
GPA4	AUX_INTERLOCK	Interlock simulator.
GPA5	SERVICE_KEY	Service input.
GPA6	POWER_MODULE_PRESENT	Presence simulator.
GPA7	FAULT_LATCH_VALID	Diagnostic input.
GPB0	BLEED_ENABLE	Low-voltage output/test LED/header only.
GPB1	FAN_ENABLE	Low-voltage output/test LED/header only.
GPB2	CONTACT_TEST_ENABLE	Low-voltage output/test LED/header only.
GPB3	FAULT_LATCH_RESET	Logic reset output.
GPB4-GPB7	MACHINE_SPARE	Spare low-voltage nets.

4.4 Keypad matrix and encoder

For each four-pin tactile switch, tie the same-side pins together: pins 1+2 to the column net and pins 3+4 to the row net, or the reverse if the footprint proves the opposite side is common. Verify with continuity on the actual switch footprint before final PCB routing.

Row / Col	KPD_COL0	KPD_COL1	KPD_COL2	KPD_COL3	KPD_COL4
KPD_ROW0	VERB	NOUN	+	-	CLR
KPD_ROW1	7	8	9	KEY REL	RSET
KPD_ROW2	4	5	6	PRO	ENTR
KPD_ROW3	1	2	3	0	SPARE
Encoder pin/function	Net	Rule			
ENC A	ENC_A	Input with pull-up; debounce/filter in firmware. Optional RC if long/noisy wiring.			
ENC B	ENC_B	Input with pull-up; quadrature B. Same debounce rules.			
ENC C/common	CMN_GND	Common side for A/B if using pull-ups.			
Switch pin 1	ENC_SW	Input with pull-up; active LOW when pressed.			
Switch pin 2	CMN_GND	Switch common to ground.			
SHIELD	PANEL_SHIELD or CMN_GND via jumper	Metal body/case. Not part of logic; helps with ESD/noise.			

4.5 U6 MCP3208 ADC, U7 REF5025 reference, U8 MCP6004 buffer

Correction that matters: MCP3208 pin 1 is CH0, not NC. Pin 14 is analog ground and pin 9 is digital ground. Tie both to the ACE logic ground, but keep analog routing local. [S3]

Pin	Name	Net	Wiring note
1	CH0	AIN0_VBANK_SIM	Pot/simulator wiper through 1 k; optional 100 nF to ground after resistor.
2	CH1	AIN1_VIN_AUX_SIM	Pot/simulator wiper through 1 k; optional 100 nF.
3	CH2	AIN2_ICHG_MON_SIM	Pot/simulator wiper through 1 k; optional 100 nF.
4	CH3	AIN3_IOUT_MON_SIM	Pot/simulator wiper through 1 k; optional 100 nF.
5	CH4	AIN4_TBANK_SIM	From U8 OUTA through 1 k; optional 100 nF.
6	CH5	AIN5_TSTAGE_SIM	From U8 OUTB through 1 k; optional 100 nF.
7	CH6	AIN6_TACE_SIM	From U8 OUTC through 1 k; optional 100 nF.
8	CH7	AIN7_THAND_SIM	From U8 OUTD through 1 k; optional 100 nF.
9	DGND	CMN_GND	Digital ground.
10	CS/SHDN	ADC_CS	Nano D10; optional 10 k pull-up so ADC is deselected at reset.
11	DIN	SPI_MOSI	Nano D11; optional 100 ohm series.
12	DOUT	SPI_MISO	Nano D12; normally no pull.
13	CLK	SPI_SCK	Nano D13; optional 100 ohm series.
14	AGND	CMN_GND	Analog ground. Tie to ground locally near ADC/reference.
15	VREF	VREF_2V5	Driven by REF5025 VOUT; local cap to ground.
16	VDD	+5V_LOGIC	Supply with 100 nF to ground.
Pin	Name	Net	Rule
1	DNC	No Connect	Do not connect. Mark with No Connect marker.
2	VIN	+5V_LOGIC	Input supply. Add 100 nF plus 1-10 uF near VIN/GND.
3	TEMP	NC or REF_TEMP_TEST	Optional temperature output/test pad. Leave NC for first bring-up.
4	GND	CMN_GND	Ground.

Pin	Name	Net	Rule
5	TRIM/NR	REF_NR	Optional 1 uF capacitor to CMN_GND for noise reduction. Mark DNP if not fitted.
6	VOUT	VREF_2V5	2.5 V reference to MCP3208 pin 15 and simulator pot top rail. Add 1-10 uF output cap to ground.
7	NC	No Connect	Leave open; mark NC. Datasheet may allow GND for layout but open is safest in schematic.
8	DNC	No Connect	Do not connect. Mark with No Connect marker.

4.6 U8 MCP6004 quad op-amp allocation

For first RevA, use each section as a unity-gain buffer for analog simulator/temp channels. A unity follower ties output back to the negative input; the signal goes into the positive input. Do not float unused op-amp inputs. [S5]

Section	Input	Input net	Feedback	ADC output path
A	pin 3 VINA+	sensor/sim input A	pin 1 OUTA tied to pin 2 VINA-	OUTA -> 1 k -> MCP3208 CH4
B	pin 5 VINB+	sensor/sim input B	pin 7 OUTB tied to pin 6 VINB-	OUTB -> 1 k -> MCP3208 CH5
C	pin 10 VINC+	sensor/sim input C	pin 8 OUTC tied to pin 9 VINC-	OUTC -> 1 k -> MCP3208 CH6
D	pin 14 VIND+	sensor/sim input D	pin 12 OUTD tied to pin 13 VIND-	OUTD -> 1 k -> MCP3208 CH7
Power	pin 11 VDD	+5V_LOGIC	pin 4 VSS -> CMN_GND	100 nF local decoupling.

4.7 U12-U14 LMV393 comparator adapters

LMV393 outputs are open-collector/open-drain style. They need pull-up resistors to create a valid HIGH. This makes them good for shared fault nets, but only if every participant on that shared net is open-drain/open-collector. [S6]

SOIC/DIP adapter pin	Name	Function	Mira rule
1	OUT1	Comparator A output	Pull up to +5V_LOGIC with 4.7 k to 10 k. May join a shared open-drain fault line.
2	IN1-	Comparator A negative input	Define with threshold or signal. Never float.
3	IN1+	Comparator A positive input	Define with signal or threshold. Never float.
4	GND	Ground	CMN_GND.
5	IN2+	Comparator B positive input	Define with signal or threshold. Never float.
6	IN2-	Comparator B negative input	Define with threshold or signal. Never float.
7	OUT2	Comparator B output	Same pull-up/open-drain rules as OUT1.
8	VCC	Power	+5V_LOGIC with 100 nF to CMN_GND.

4.8 U9 ULN2803A LED driver and talkback outputs

The ULN2803A is an eight-channel low-side sink. It does not source +5 V. The load goes from +5 V through its resistor/load into the ULN output. COM is for inductive clamp diodes; for LEDs only, COM can be NC. [S9]

Pin	Name	Net/load	Wiring note
1	IN1	TB_SAFE_CMD	From U4 output
2	IN2	TB_CHARGE_CMD	From U4 output
3	IN3	TB_READY_CMD	From U4 output
4	IN4	TB_ARMED_CMD	From U4 output
5	IN5	TB_OUTPUT_CMD	From U4 output
6	IN6	TB_FAULT_CMD	From U4 output
7	IN7	TB_ENERGY_CMD	From U4 output
8	IN8	TB_OPR_ERR_CMD	From U4 output
9	GND/E	CMN_GND	Emitter/common ground
10	COM	NC for LEDs	Connect to +V only for inductive loads requiring clamp diodes
11	OUT8	OPR_ERR LED cathode	+5V -> 1 k -> LED -> OUT8
12	OUT7	ENERGY LED cathode	+5V -> 1 k -> LED -> OUT7
13	OUT6	FAULT LED cathode	+5V -> 1 k -> LED -> OUT6

Pin	Name	Net/load	Wiring note
14	OUT5	OUTPUT LED cathode	+5V -> 1 k -> LED -> OUT5
15	OUT4	ARMED LED cathode	+5V -> 1 k -> LED -> OUT4
16	OUT3	READY LED cathode	+5V -> 1 k -> LED -> OUT3
17	OUT2	CHARGE LED cathode	+5V -> 1 k -> LED -> OUT2
18	OUT1	SAFE LED cathode	+5V -> 1 k -> LED -> OUT1

Buzzer note: if all eight ULN channels are used by the talkback LEDs, do not overload an expander pin directly. Add a separate small NPN/MOSFET low-side buzzer driver or reserve/reassign a ULN channel.

4.9 U10 SN74HC573A fault latch

The SN74HC573A is an octal transparent latch with 3-state outputs. It is not open-drain. Define OE and LE. Do not tie its outputs together with other push-pull outputs. Tie unused inputs to a defined logic level. [S8]

Pin(s)	Name	Function	Mira rule
1	OE	Output enable	Define explicitly. Often tie LOW to enable outputs, or drive from a control net if you need tri-state.
2-9	1D-8D	Data inputs	Fault-source bits or test inputs. Tie unused inputs high/low; never float.
10	GND	Ground	CMN_GND.
11	LE	Latch enable	Define explicitly. HIGH transparent; LOW holds latched value.
12-19	8Q-1Q	Outputs	Push-pull/3-state. Route to diagnostic inputs, not shared wires.
20	VCC	Power	+5V_LOGIC with 100 nF decoupling.

4.10 U11 CD74HC221 logic-only timing/window fixture

The CD74HC221 is a dual monostable. It is useful as a low-voltage timing/window test fixture, not as output-stage construction guidance. Its Q outputs are CMOS outputs, not open-drain. Unused inputs must not float. [S7]

Pin	Name	Function	Mira rule
1	1A	Trigger input	Bias/drive to defined state.
2	1B	Trigger input	Bias/drive to defined state.
3	1R	Reset	Define; reset terminates pulse.
4	1Qbar	Complement output	Push-pull output; do not wire-OR.
5	2Q	Output	Push-pull output.
6	2Cx	Timing capacitor pin	Use only in datasheet timing network.
7	2CxRx	Timing RC pin	Use only in datasheet timing network.
8	GND	Ground	CMN_GND.
9	2A	Trigger input	Bias/drive to defined state.
10	2B	Trigger input	Bias/drive to defined state.
11	2R	Reset	Define; reset terminates pulse.
12	2Qbar	Complement output	Push-pull output; do not wire-OR.
13	1Q	Output	Push-pull output.
14	1Cx	Timing capacitor pin	Use only in datasheet timing network.
15	1CxRx	Timing RC pin	Use only in datasheet timing network.
16	VCC	Power	+5V_LOGIC with 100 nF decoupling.

5. Plain-English Concepts

5.1 Pull-up vs pull-down

Pull-up: default HIGH

```
+5V_LOGIC
|
[10k]
|
SIGNAL ----> input pin
|
switch
|
CMN_GND
```

switch open -> HIGH
switch closed -> LOW (active-low input)

Pull-down: default LOW

```
+5V_LOGIC
|
switch
|
SIGNAL ----> input pin
|
[10k]
|
CMN_GND
```

switch open -> LOW
switch closed -> HIGH (active-high input)

For most ACE switches, use **pull-up + switch to ground**. It behaves a lot like inverted redstone/torch logic: the default state is HIGH, and pressing/closing the switch pulls it LOW.

5.2 Open-drain / open-collector vs push-pull

Open-drain/open-collector shared line

```
+5V_LOGIC
|
[4.7k or 10k pull-up]
|
FAULT_SUM / EXPANDER_INT ----> Nano input
|
+---- LMV393 output (can pull low)
+---- MCP23017 INT in ODR (can pull low)
+---- another OD fault (can pull low)
```

No device drives HIGH. The resistor creates HIGH.
Any device can pull LOW without fighting another device.

Push-pull output

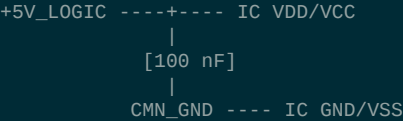
logic output ----> one input

The output actively drives HIGH and LOW.
Do not tie two push-pull outputs to the same wire.
Examples: normal GPIO outputs, SN74HC573 Q outputs, CD74HC221 Q outputs.

Use case	Use this	Reason
One output drives one input	Push-pull	Simpler and faster. No pull-up required.
Several fault/interrupt sources share one Nano input	Open-drain/open-collector plus one pull-up	Any device can assert LOW without output contention.
I2C bus	Open-drain style plus pull-ups	I2C devices pull the bus LOW and release it HIGH.
LMV393 output	Open-collector plus pull-up	The part cannot drive HIGH by itself.
ULN2803A LED outputs	Low-side sink	This is for current sinking through loads, not a shared logic bus.

5.3 Decoupling capacitors

A 100 nF decoupling capacitor goes between an IC power pin and ground, physically close to the IC. It is not a short at DC; it is a tiny local energy pool for fast current gulps and a high-frequency noise shunt.



5.4 VREF and analog range

The REF5025 creates `VREF_2V5`. That net is the measuring ruler for the MCP3208. With `VREF` at 2.5 V, an ADC input should stay between 0 V and 2.5 V. Use dividers/buffers/protection before real external signals ever reach the ADC.

5.5 NC, DNC, unused, and DNP

Label	Meaning	How to handle in KiCad
NC	No Connect	Leave open and place a No Connect marker unless datasheet allows a defined tie.
DNC	Do Not Connect	Treat more strictly than NC: leave open. Do not use as a convenient via/wire anchor.
Unused input	Pin function exists but you are not using it	Tie to a defined HIGH or LOW, or bias through a resistor. Do not float.
Unused output	Output you are not reading	Can often be left unconnected if datasheet permits.
DNP	Do Not Populate	Footprint exists on schematic/PCB, but leave the physical component uninstalled for now.

6. KiCad and ERC Guidance

KiCad ERC is not a judge of your design intent. It is a warning system. Fix power shorts and output-output fights first; suppress intentional warnings only after verifying the circuit behavior.

ERC symptom	What it usually means	Fix
Power pin not driven	KiCad sees VDD/VCC/VREF but no power source	Add PWR_FLAG on +5V_LOGIC and CMN_GND. For VREF_2V5, confirm REF5025 VOUT drives it; add No ERC only if needed after confirming.
Multiple net names on one wire	Two labels/power symbols define same copper differently	Pick one net name. Use CMN_GND everywhere or GND everywhere, not both.
Output connected to output	Two push-pull drivers fight	Do not join push-pull outputs. Open-drain outputs can share only if all participants are OD/OC and the net has a pull-up.
Input pin not driven	Input may float	Add pull-up/pulldown, tie to a defined logic level, or mark No ERC only after confirming it is handled internally.
Pin not connected	KiCad sees an unconnected pin	For genuine NC/DNC, add No Connect marker. For unfinished blocks, ignore temporarily but track before PCB.
Dangling label	Text looks connected but the label anchor is not on a wire/pin	Move label until it snaps; highlight net or wiggle wire to confirm.
Open-drain missing pull-up	Electrical behavior undefined even if schematic connects	Add 4.7 k or 10 k pull-up to +5V_LOGIC.
COM pin on ULN	Often mistaken for ground	COM is clamp diode common; leave NC for LEDs only, connect to load +V for inductive loads.

Breadboard-readable schematic style

Inside a block	Between blocks
Use visible straight local wires so you can trace chip pin -> resistor/cap -> next chip pin.	Use net labels for long-distance bus nets like I2C_SDA, SPI_SCK, FAULT_SUM.
Keep the keypad matrix, LED driver chains, ADC/reference, and op-amp buffers visibly wired.	Do not drag diagonal wires across the whole sheet.
Use bus graphics for obvious bundles like KPD_ROW[0..3] if they help readability.	Do not hide safety-critical lines like HARD_SAFE_SW or FAULT_SUM in a confusing bus.

7. Must-Connect / Optional / Leave-Open Checklist

Device	Must connect	Recommended	Optional	Leave open / caution
Nano Every	+5V, GND, bus pins you use, direct safety pins	TX/RX service header	Unused analog/GPIO pins, AREF if external ADC only	None of the used pins
MCP23017	VDD, VSS, SDA, SCL, A0/A1/A2, RESET	INTA/INTB, 100 nF	Internal weak pull-ups for short local inputs	Pins 11 and 14 NC
MCP3208	VDD, DGND, AGND, VREF, CS, DIN, DOUT, CLK, used channels	100 nF, local analog routing	Unused channels may be left unused or tied gently	No NC pin on MCP3208 PDIP-16; pin 1 is CH0
REF5025	VIN, GND, VOUT	VIN bypass, NR cap, output cap	TEMP test pad	DNC pins 1/8; NC pin 7
MCP6004	VDD, VSS, every used op-amp input/output	100 nF; follower feedback	Spare channels if biased sanely	Do not float used inputs
LMV393	VCC, GND, comparator inputs, output pull-up	100 nF	Shared open-drain fault net	Do not float inputs
CD74HC221	VCC, GND, used A/B/R, timing pins	Defined states on unused inputs	Second channel if not needed	Do not float unused inputs
SN74HC573A	VCC, GND, OE, LE, used D/Q	Tie unused inputs	Unused outputs may remain open	Do not float OE/LE/inputs
ULN2803A	GND, used inputs, used outputs	COM for inductive loads	Unused channels	COM NC for LEDs only is OK
FRAM breakout	VCC, GND, SDA, SCL	WP low, A pins strapped	WP control later	Do not leave represented address pins floating
PEC11R encoder	A, B, common	Pull-ups and debounce	SHIELD to PANEL_SHIELD	A/B must not float
TPD4E05U06	Only when protected connector lines exist	Near connector entry	Skip earliest breadboard stage	N/A
SMBJ5.0A	Across 5 V entry rail when fitted	Near rail entry	Skip earliest minimal bench lash-up if desired	N/A

8. Breadboard Bring-up Order

Step	Block	Pass condition
1	Rail sanity	Verify +5V_LOGIC and CMN_GND only. No ICs inserted if using sockets.
2	Nano + serial	Boot Nano; confirm service UART/USB serial logs.
3	I2C pull-ups	Install 4.7 k SDA/SCL pull-ups; run I2C scanner with no devices, then one device.
4	FRAM	Add U2; verify 0x50 and read/write test.
5	One MCP23017	Add U3 only; verify address straps and simple GPIO input/output.
6	Remaining expanders	Add U4 then U5; verify addresses 0x21 and 0x22.
7	Keypad/encoder	Scan one row/column block; confirm active-low behavior and debounce.
8	SPI ADC	Add MCP3208; confirm SPI returns stable raw values.
9	Reference	Add REF5025; verify VREF_2V5, then ADC counts against known voltages.
10	Analog simulator	Add pots and MCP6004 buffers one channel at a time.
11	LED driver	Add ULN2803 and one LED chain; then add all talkbacks.
12	Fault logic	Add LMV393 pull-ups/shared fault net; then latch/monostable blocks.
13	Protection	Add TVS/ESD placeholders on a PCB/perfboard build, not as fragile breadboard-first essentials.

9. Source References

These are the primary documents used to build this reference. Datasheet citations are shown as [S#] throughout the document.

ID	Source	URL / file
S1	Arduino Nano Every ABX00028 datasheet, Arduino docs.	https://docs.arduino.cc/resources/datasheets/ABX00028-datasheet.pdf
S2	Microchip MCP23017 data sheet.	https://ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/MCP23017-Data-Sheet-DS20001952.pdf
S3	Microchip MCP3208 data sheet.	https://ww1.microchip.com/downloads/aemDocuments/documents/APID/ProductDocuments/DataSheets/21298e.pdf
S4	Texas Instruments REF50xx data sheet.	https://www.ti.com/lit/gpn/ref50
S5	Microchip MCP6001/2/4 family data sheet.	https://ww1.microchip.com/downloads/aemDocuments/documents/MSLD/ProductDocuments/DataSheets/MCP6001-1R-1U-2-4-1-MHz-Low-Power-Op-Amp-DS20001733L.pdf
S6	Texas Instruments LMV393 data sheet/product documentation.	https://www.ti.com/product/LMV393
S7	Texas Instruments CD74HC221 data sheet.	https://www.ti.com/lit/gpn/cd74hc221
S8	Texas Instruments SN74HC573A data sheet.	https://www.ti.com/lit/gpn/sn74hc573a
S9	STMicroelectronics ULN2803A data sheet.	https://www.st.com/resource/en/datasheet/uln2803a.pdf
S10	Adafruit I2C FRAM breakout 1895 pinouts and product documentation.	https://learn.adafruit.com/adafruit-i2c-fram-breakout/pinouts
S11	Bourns PEC11R encoder data sheet.	https://www.bourns.com/docs/product-datasheets/pec11r.pdf
S12	Texas Instruments TPD4E05U06 ESD array documentation.	https://www.ti.com/product/TPD4E05U06
S13	NanoArc ACE RevA BOM, missing BOM, DigiKey invoice, and architecture baseline supplied by user.	Uploaded project files: BOM PDFs, DK_INVOICE_128473475.pdf, and NanoArc architecture baseline.

Revision note: This PDF is intended to replace the earlier table-only pinmap as the bench reference. Keep the earlier PDF as historical context if you want, but use this document for datasheet-specific warnings and explanations.